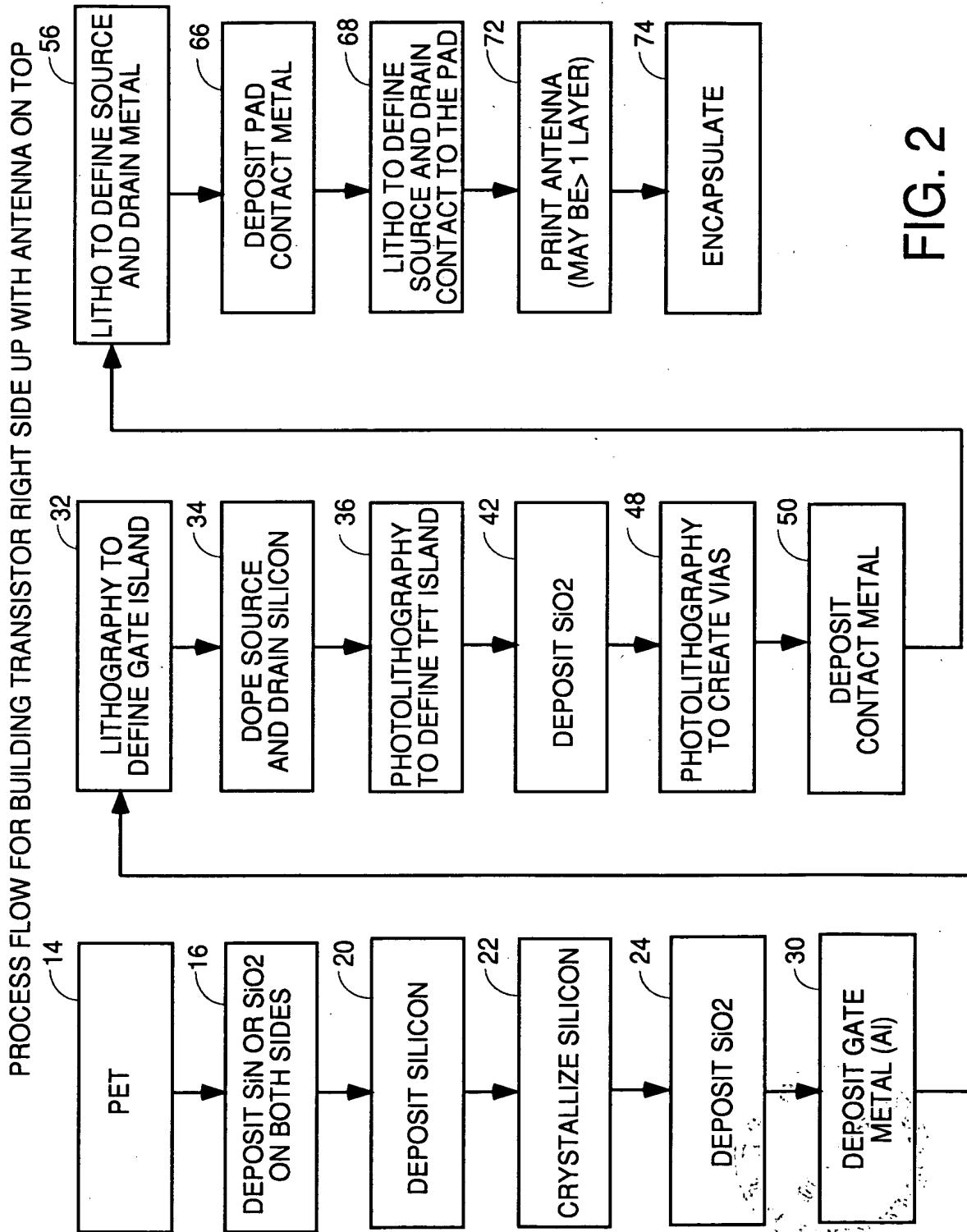


FIG. 1



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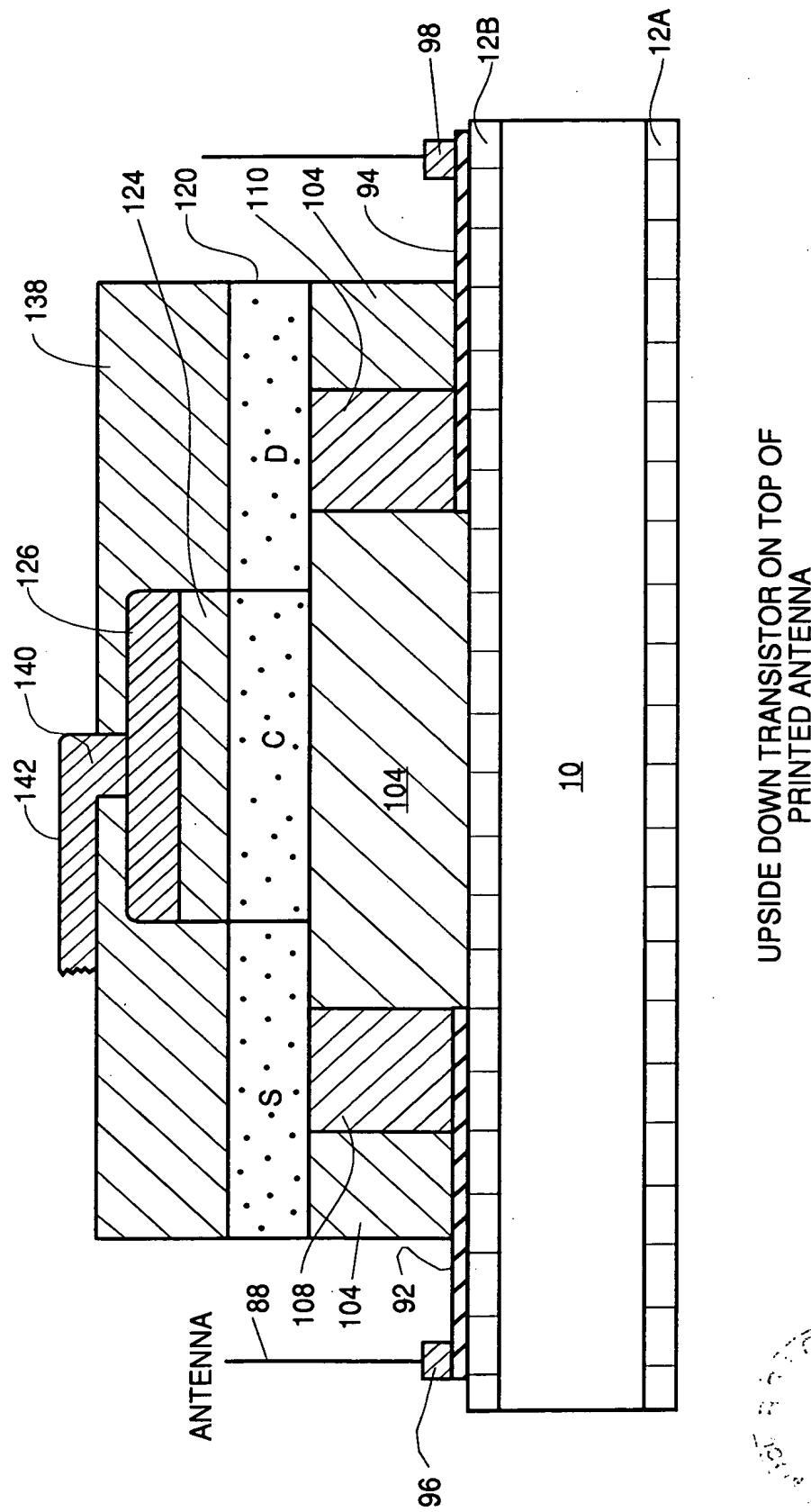


FIG. 3

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PROCESS FLOW FOR BUILDING TRANSISTOR ON TOP OF ANTENNA

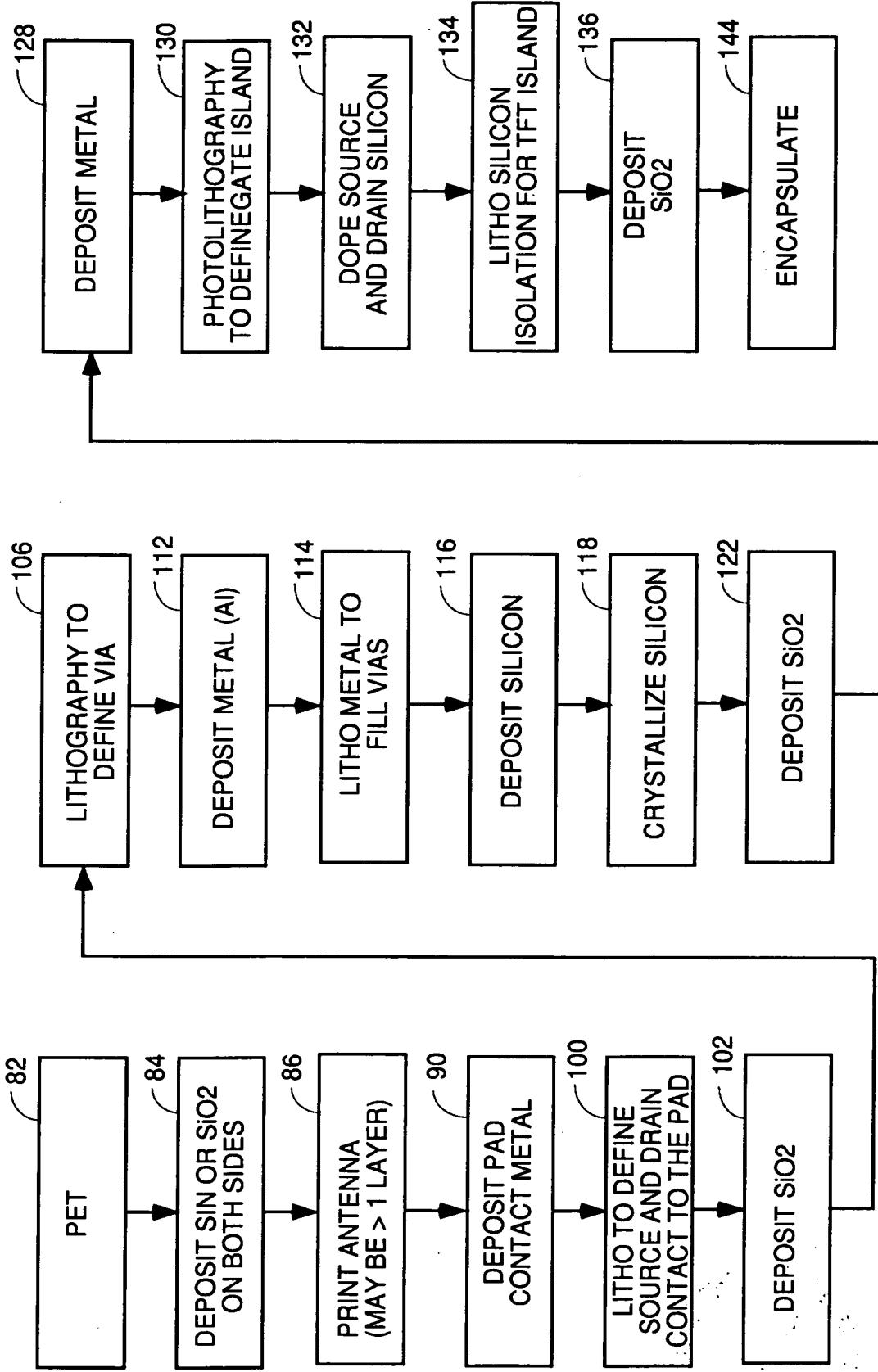


FIG. 4

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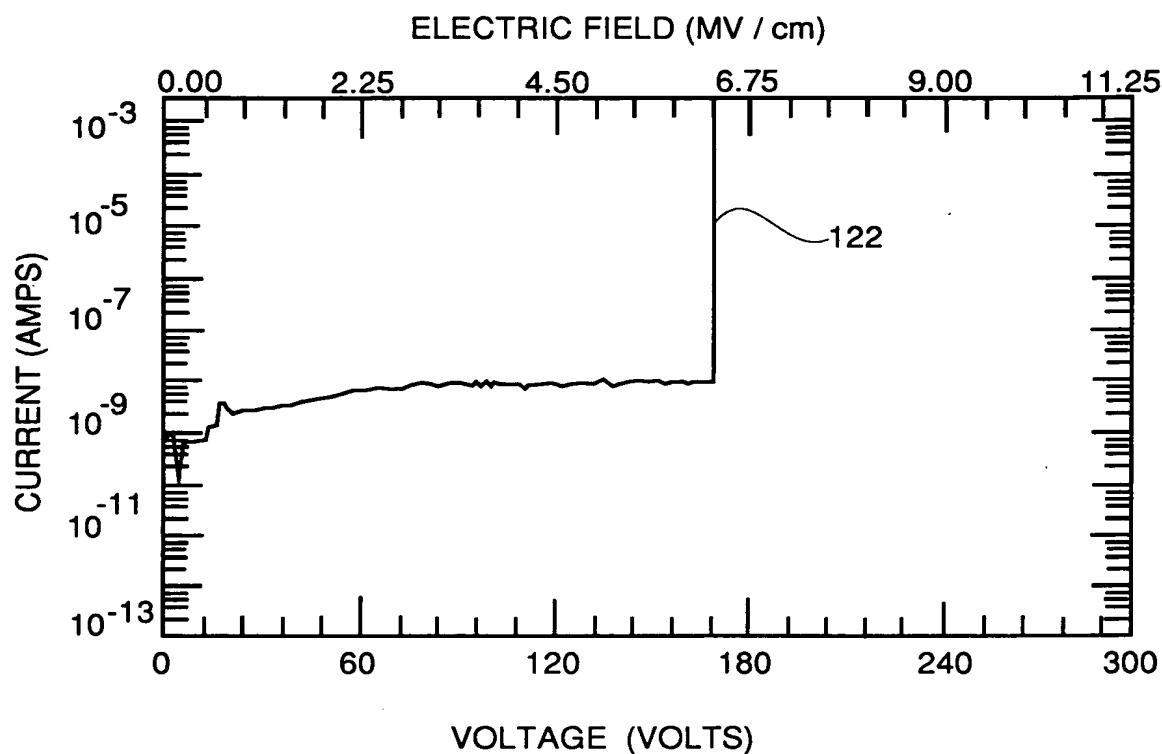


FIG. 5

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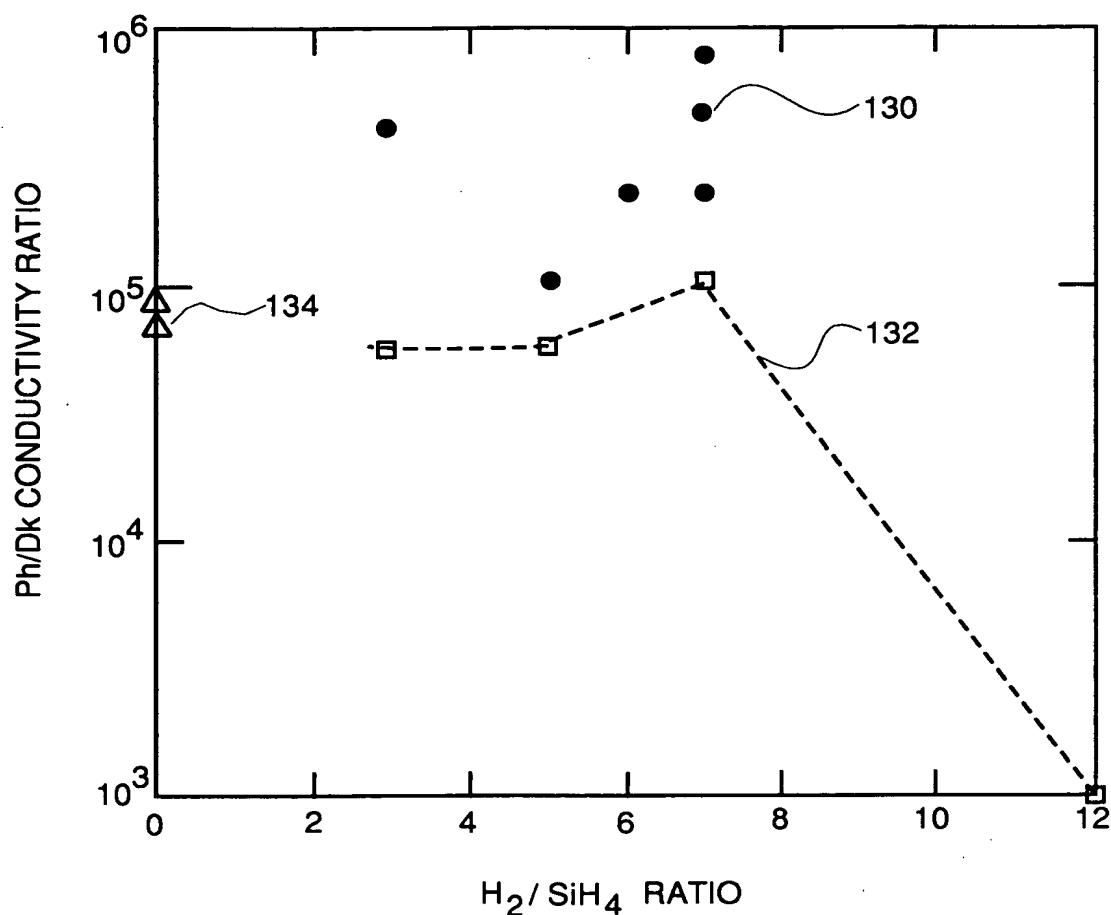


FIG. 6

PROCESS FLOW FOR BUILDING EEPROM WITH ANTENNA ON TOP

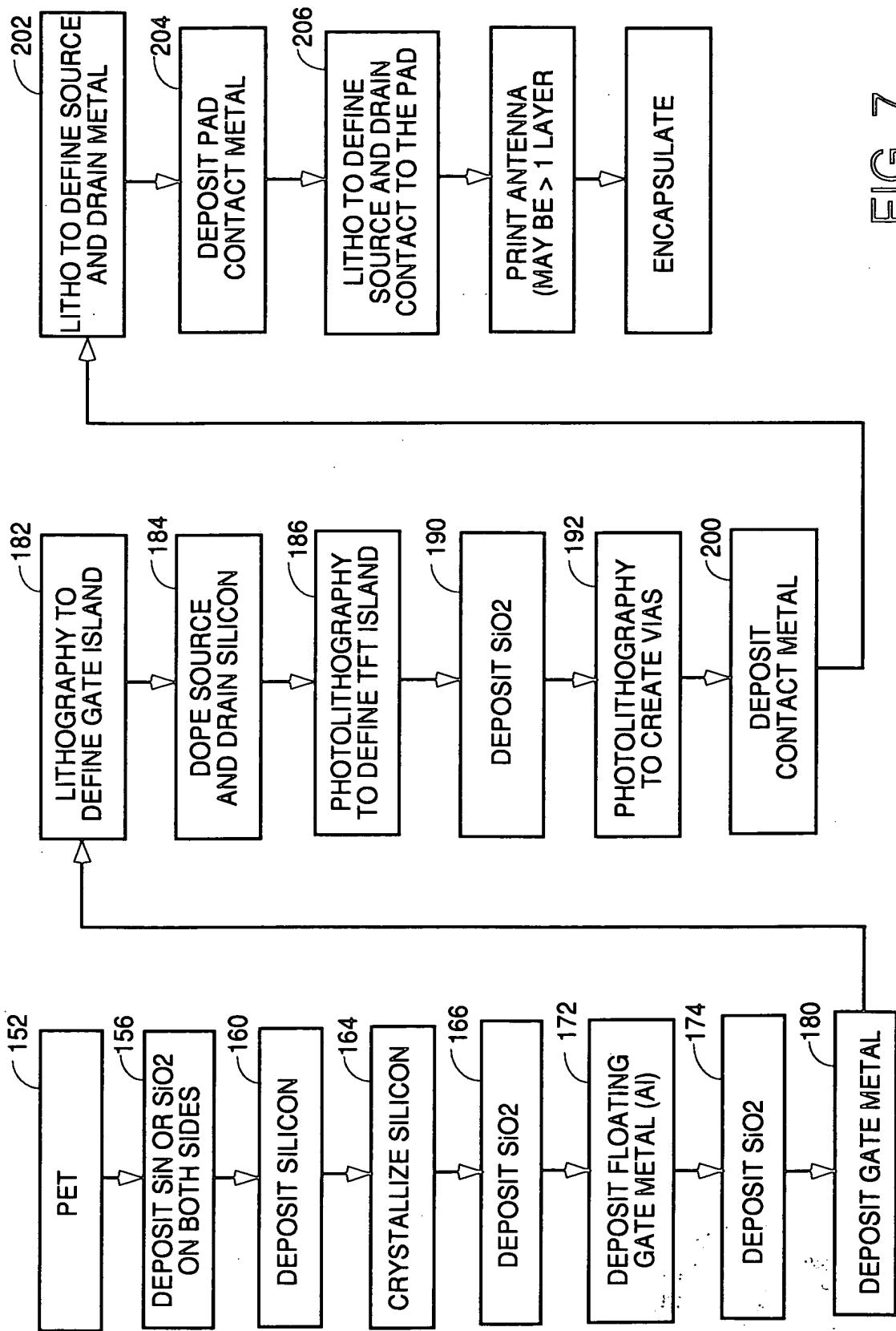
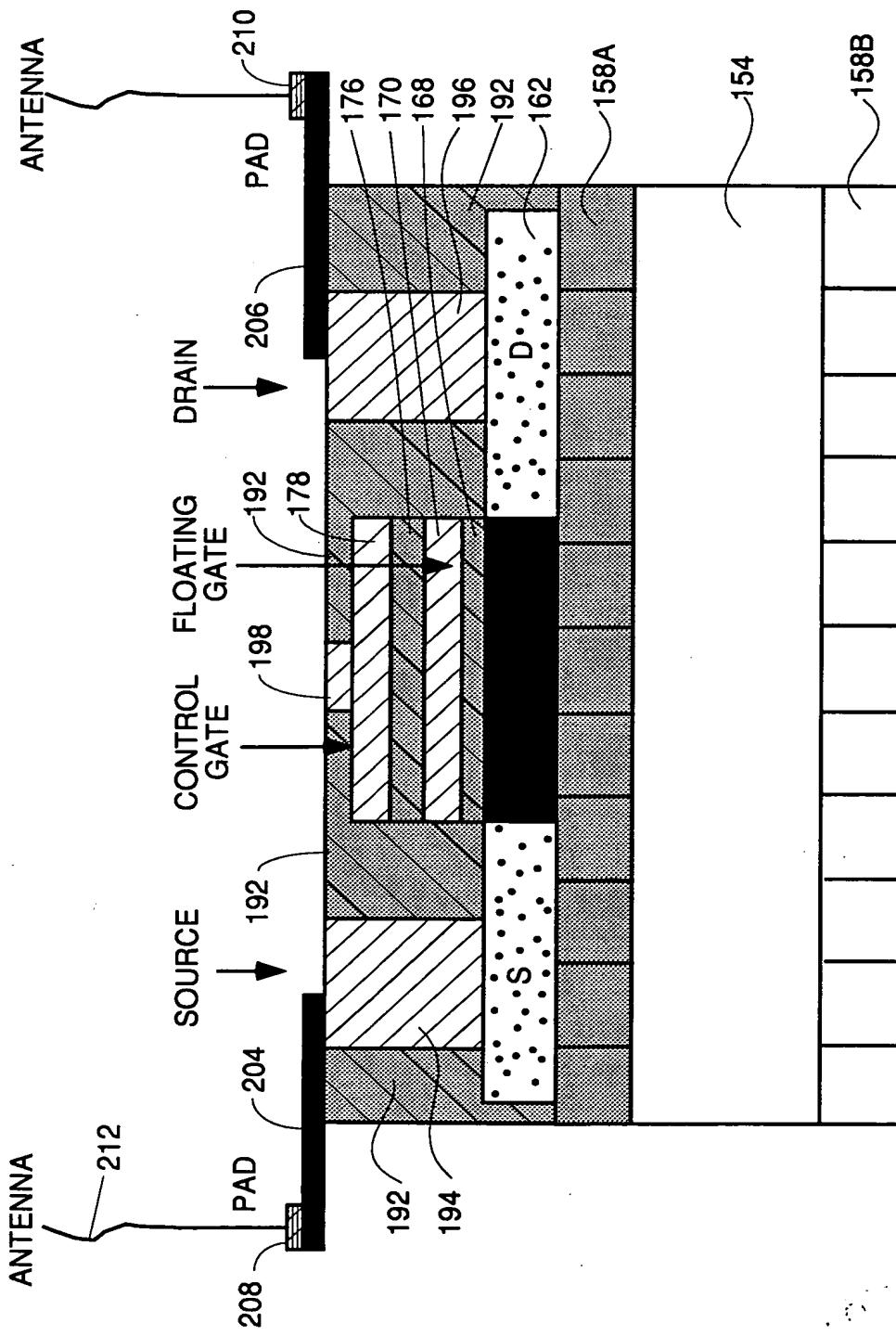


FIG. 7



SCHEMATIC OF A SINGLE EEPROM BUILT ON PET WITH THE CONTACT PADS AND THE ANTENNA PRINTED ON TOP OF THE TRANSISTOR; GATE WILL BE CONNECTED TO THE TRANSISTORS (IN ACTUAL DEVICES MULTIPLE TRANSISTORS AND EEPROM WILL BE CONNECTED TO THE CONTACT PADS)

FIG. 8

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PROCESS FLOW FOR BUILDING EEPROM ON TOP OF ANTENNA

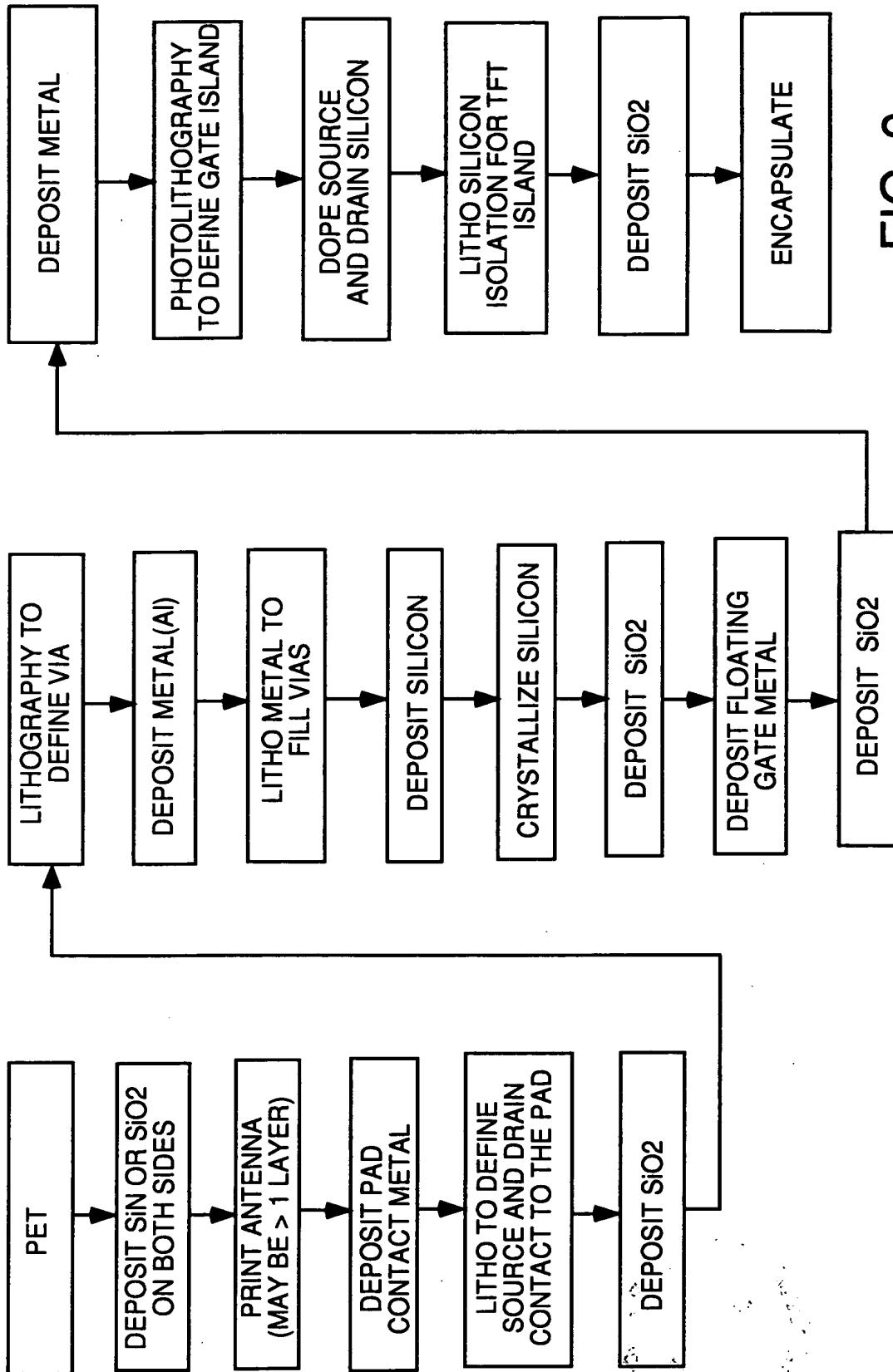
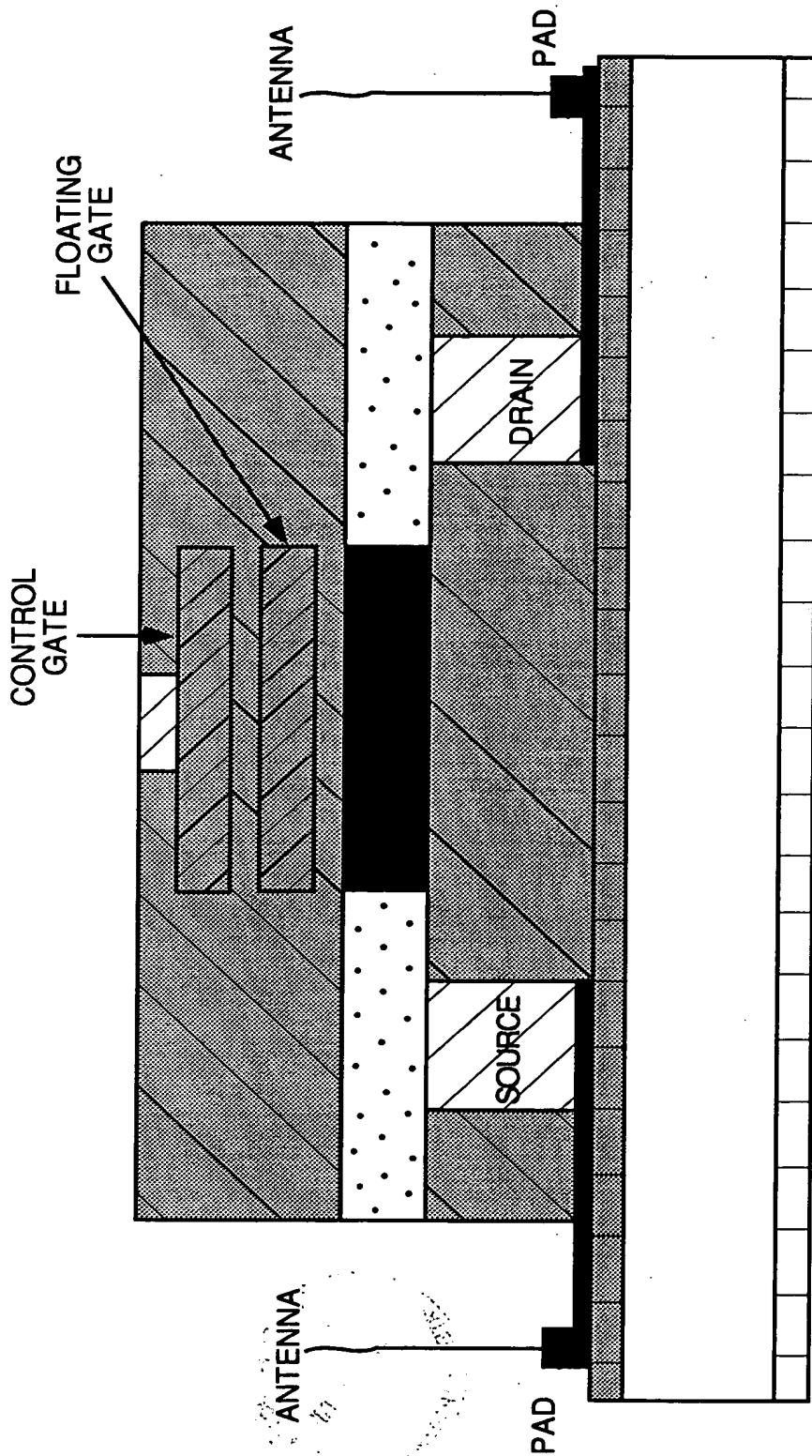


FIG. 9

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SCHEMATIC OF A SINGLE EEPROM BUILT ON TOP OF THE PRINTED ANTENNA
(IN ACTUAL DEVICES EEPROM AND MULTIPLE TRANSISTORS WILL BE CONNECTED TO THE CONTACT PADS)

FIG. 10